

DESIGN OF A LOW POWER MULTIBAND CLOCK DISTRIBUTION CIRCUIT USING SINGLE PHASE CLOCK

T.BhavyaBhavani⁽¹⁾, Dr.K.Seshadri Sastry⁽²⁾, Dr.G.R.L.V.N Srinivas Raju⁽³⁾

T.BhavyaBhavani⁽¹⁾, M.Tech student -VLSI Design, Dept of ECE, Shri Vishnu Engg College for Women

Dr.K.Seshadri Sastry⁽²⁾, Professor, Dept of ECE, Shri Vishnu Engineering College for Women

Dr.G.R.L.V.N Srinivas Raju⁽³⁾, Professor and H.O.D, Dept of ECE, Shri Vishnu Engg College for Women

ABSTRACT:

The clock distribution network consumes nearly 70% of the total power consumed by the integrated circuit since this is the only signal which has the highest switching activity. Normally for a multiband clock domain network we develop a multiple PLL to cater the need. This project aim for developing a low power true single phase clock(TSPC) multiband network which will supply for the multi clock domain network. In this paper, a wide band 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 or 64/65/78/79 prescaler. A dynamic logic multiband flexible integer-n divider based on pulse swallow topology is proposed which uses a low power wide band 2/3 prescaler and a wide band multimodulus 32/33/47/48 or 64/65/78/79 prescaler. Since the multimodulus 32/33/47/48 or 64/65/78/79 prescaler has a maximum operating frequency of 6.2GHz, the values of P and S counters can actually be programmed to divide over the whole range of frequencies. However the P and S counter are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit cell for swallow counter and consumes a power of 0.96 and 2.2mW. This project is highly useful and recommended for communication applications like Bluetooth, Zigbee, IEEE 802.15.4 and 802.11 a/b/g WLAN frequency synthesizers which are proposed based on pulse swallow topology. This design is modelled using Verilog simulated tool 'MODELSIM 6.4b' and implemented and synthesized using 'Xilinx ISE 10.1'.

Keywords: True single phase clock (TSPC), Frequency synthesizer, Multimodulus prescaler, Phase locked loop (PLL)

I. INTRODUCTION

Wireless LAN (WLAN) in the multi gigahertz bands, such as HIPER LAN II and Network standards like 802.11a/b/g are recognized as leading standards for high-rate data transmissions, and standards like Network protocol 802.15.4 are recognized for low-rate data transmissions. The integrated synthesizers for Wireless LAN applications at 5 GHz reported in and consume up to 24 mw in CMOS realizations, where the first-stage divider is implemented using an Injection-locked divider which consumes large chip area and has a narrow locking range. The best published frequency synthesizer at 5 GHz consumes 9.6 mw at 1-V supply, where its complete divider consumes power around 6 mw, where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating Frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers.

High speed divide-by- counter (also called prescaler) is a fundamental module for frequency synthesizers. Its design is crucial because it operates at a higher frequency and consumes higher power consumption. A divide-by- counter consists of flip-

flops (FF) and extra logic, which determines the terminal count. Conventional high speed FF based divide by counter designs use current-mode logic (CML) latches and suffer from the disadvantage of large load capacitance. This not only limits the maximum operating frequency and current-drive capabilities, but also increases the total power consumption. Alternatively, FF based divide-by designs adopt dynamic logic FFs such as true-single-phase clock (TSPC). The designs can be further enhanced by using extended true-single-phase-clock (E-TSPC) FFs for high speed and low power applications. E-TSPC designs remove the transistor stacked structure so that all the transistors are free of the body effect. They are thus more sustainable for high operating frequency operations in the face of low voltage supply. Past optimization efforts on prescaler designs focused on simplifying the logic part to reduce the circuit complexity and the critical path delay. For example, an E-TSPC design embedded with one extra P-MOS/N-MOS transistor can form an integrated function of FF and AND/OR logic. Moving part of the control logic to the first FF to reduce unnecessary FF toggling yields another version of prescaler design .These two classic designs

each contains 16 transistors only and the mode control logic uses as few as 4 transistors. To achieve such circuit simplicity, it calls for a rationed structure in the FF design. Despite its distinct speed performance, the incurred static and short circuit power consumptions are significant. Latest designs presented in adopt a general TSPC logic family containing both rationed and ratio less inverter alternatives. Since the maximum height of transistor stacking is up to 5, these designs lose their performance advantages when working under a low scenario. In a power gating technique by inserting an extra PMOS between and the FF is employed in two novel divide-by-2/3 counter designs. The unused FF can be shut down when working in the divide-by-2 mode. Due to the increase in the number of transistor stacking (up to 4), these designs are not suitable for low operations. Due to the quadratic dependence of power consumption on supply voltage, lowering is a very effective measure to reduce the power at the expense of speed performance. In particular, here focus on low operations for power saving without sacrificing the speed performance. In this design, rationed E-TSPC FFs are employed due to its circuit simplicity and speed performance. Only one pass transistor is needed to implement the mode control logic. The proposed design in capable of working at a maximum frequency of 531 MHz when the supply voltage is as low as 0.6 V.

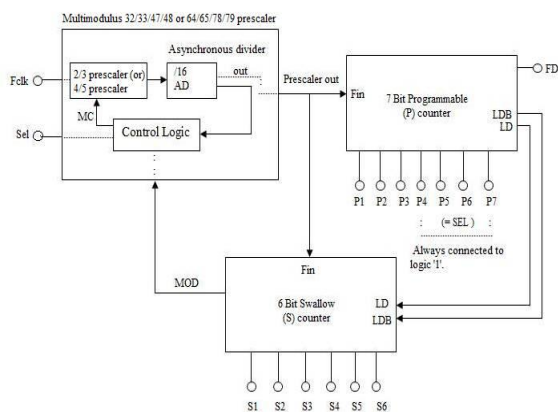


Fig 1: Proposed dynamic logic multiband flexible divider.

The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5 GHz. The frequency synthesizer reported in [6] uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.25 mw. Most Network protocol 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage, while dynamic latches are

not yet adopted for multiband synthesizers. In this paper, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multi modulus 32/33/47/48 prescaler as shown in Fig. 1. The divider also uses an improved low power loadable bit-cell for the Swallow-counter.

II. DESIGN CONSIDERATIONS

The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated and is given by

$$f_{\max} = 1/(t_{pLH} + t_{pHL})$$

Where t_{pLH} and t_{pHL} are the propagation delays of gates, respectively. The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{\text{Switching}} = \sum_{i=1}^n f_{\text{clk}} C_{Li} V_{dd}^2$$

where n is the number of switching nodes f_{clk} is the clock frequency C_{Li} is the load capacitance at the output node of the stage, and V_{dd} is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{\text{sc}} = I_{\text{sc}} * V_{dd}$$

where I_{sc} is the short-circuit current. The analysis in shows that the short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18- μm CMOS process.

III. WIDEBAND E-TSPC 2/3 PRESCALER

The E-TSPC 2/3 prescaler consumes large short circuit power and has a higher frequency of operation than that of TSPC 2/3 prescaler. The wideband single-phase clock 2/3 prescaler used in this design consists of two D-flip-flops and two NOR gates embedded in the flip flops. The first NOR gate is

embedded in the last on DFF1, and the second NOR gate is embedded in the first stage of DFF2.

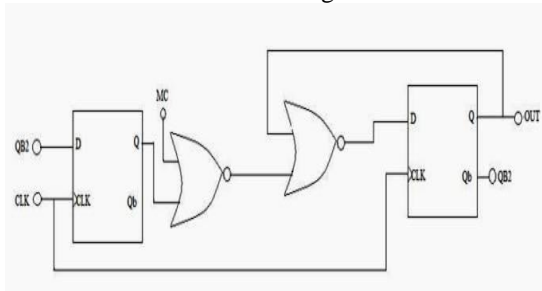


Fig 2: Wideband single-phase clock 2/3 prescaler.

The first NOR gate is embedded in the last stage of DFF1, and the second NOR gate is embedded in the first stage of DFF2. The switching of division ratios between 2 and 3 is controlled by logic signal MC.

When logic signal MC switches from "1" to "0", the logic value at the input of DFF1 is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is "0" and the wideband prescaler operates at the divide-by-3 mode. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1. Thus, the wideband 2/3 prescaler has benefit of saving more than 50% of power during the divide-by-2 operation. The measured results shows that the wideband 2/3 prescaler has the maximum operating frequency of 6.5GHz.

IV. MULTIMODULUS 32/33/47/48 or 64/65/78/79 PRESCALER

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47 and 48 or 64, 65, 78 and 79 is shown in Fig. 3. It is similar to the 32/33 or 64/65 prescaler used in, but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48 or divide-by-78 and divide-by-79) without any extra flip flop, thus saving a considerable amount of power and also reducing the complexity of multi band divider.

The multimodulus prescaler consists of the wideband 2/3 ($N_1/(N_1+1)$) prescaler, four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios.

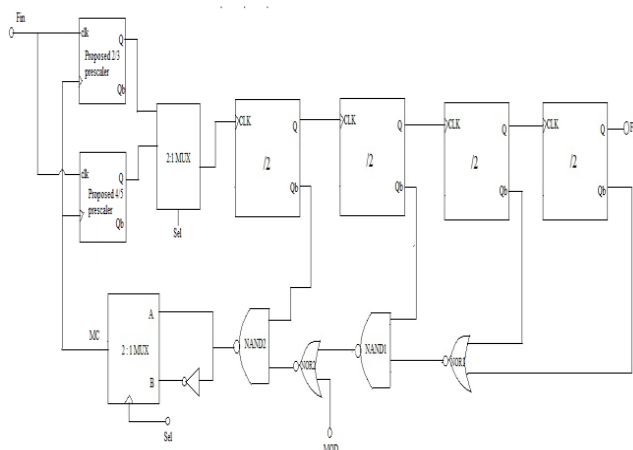


Fig 3: Proposed Multimodulus 32/33/47/48 (or) 64/65/78/79 Prescaler

Beside the usual MOD signal for controlling $N/(N+1)$ divisions, the additional control signal sel is used to switch the prescaler between 32/33 and 47/48 modes.

1) Case 1: sel='0'

When sel='0', the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC=0, the 2/3 prescaler operates in the divide-by-3 mode. If MOD=1, the NAND2 gate output switches to logic "1" (MC=1) and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multi modulus prescaler is

$$N = (AD * N_1) + (0 * (N_1 + 1)) = 32$$

Where $N_1=2$ and $AD=16$ is fixed for the entire design. If MOD = 0, for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the Divide-by-3 mode. The division ratio $N+ 1$ performed by the multi modulus prescaler is

$$N+1 = ((AD - 1) * N_1) + (1 * (N_1 + 1)) = 33$$

2) Case 2: sel = '1'

When sel='1', the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operate as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC= 1, the 2/3 prescaler operates in divide-by- 3 mode and when MC=0, the

2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when sel='0' If MOD=1, the division ratio N+ 1 performed by the multimodulus prescaler is same except that the wideband prescaler operates in the divide by-3 mode for the entire operation given by

$$N + 1 = (AD * (N_1+1)) + (0 * N_1) = 48$$

If MOD=1, the division ratio N performed by the multimodulus prescaler is

$$N = ((AD - 1) * (N_1 + 1)) + (1 * N_1)=47.$$

In order to get 64/65/78/79 clock cycles we need to operate 4/5 prescaler by making the control signal sel of second MUX to '1'. To get 32/33/47/48 prescaler, the second MUX should be equal to '0' means the control signal sel of the second MUX should be equal to '0' and to get 64/65/78/79 prescaler, the second MUX should be equal to '1' means the control signal sel of the second MUX should be equal to '1'.

1) Case 1: sel='0'

When sel='0', the output from the NAND2 gate is directly transferred to the input of 4/5 prescaler and the multimodulus prescaler operates as the normal 64/65 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 4/5 prescaler operates in the divide-by-2 mode and when MC = 0, the 4/5 prescaler operates in the divide-by-3 mode. If MOD=1, the NAND2 gate output switches to logic "1" (MC=1) and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multi modulus prescaler is

$$N = (AD*N_1) + (0*(N_1 + 1)) = 64$$

Where $N_1=2$ and $AD=16$ is fixed for the entire design. If MOD = 0, for 62 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the Divide-by-3 mode. The division ratio N+ 1 performed by the multi modulus prescaler is

$$N+1 = ((AD - 1)*N_1) + (1 * (N_1 + 1)) = 65$$

2) Case 2: sel = '1'

When sel=' 1', the inverted output of the NAND2 gate is directly transferred to the input of 4/5 prescaler and the multimodulus prescaler operate as a 64/65 prescaler, where the division ratio is controlled by the logic signal MOD. If MC= 1, the 4/5 prescaler operates in divide-by- 3 mode and when MC=0, the 4/5 prescaler operates in divide-by-2 mode which is

quite opposite to the operation performed when sel='0' If MOD=1, the division ratio N+ 1 performed by the multimodulus prescaler is same except that the wideband prescaler operates in the divide by-3 mode for the entire operation given by

$$N + 1 = (AD * (N_1+1)) + (0 * N_1) = 79$$

If MOD=1, the division ratio N performed by the multimodulus prescaler is

$$N = ((AD - 1) * (N_1 + 1)) + (1 * N_1)=78.$$

V. MULTIBAND FLEXIBLE DIVIDER

The single-phase clock multiband flexible divider which is shown in Fig 1 consists of the multi modulus 32/33/47/48 or 64/65/78/79 prescaler, a 7-bit programmable (P) counter and a 6-bit swallow(S) counter. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5-5.825 GHz).

I. Swallow (S) Counter

The 6-bit s-counter shown in Fig.4 consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 or 0 to 63 for low-frequency band and from 0 to 47 or 0 to 78 for the high-frequency band. The asynchronous bit cell used in this design .It is similar to the bit-cell except it uses two additional transistors M6 and M7 whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S1 (divide-by-48 or divide-by-79) and P, S counters start down counting the input clock cycles. When the S-counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-n mode (divide-by-32 or divide-47 or divide-by-64 or divide-78) for the remaining P-S clock cycles. During to a specified value from 0 to 31 or 0 to 63 for the lower band and 0 to 48 or 0 to 79 for the higher band of operation. this mode, since S-counter is idle, transistors M6 and M7 which are controlled by MOD, keep the nodes S1 and S2 at logic "0," thus saving the switching power in S counter for a period of (N*(P-S)) clock cycles. Here, the programmable input (PI) is used to load the counter.

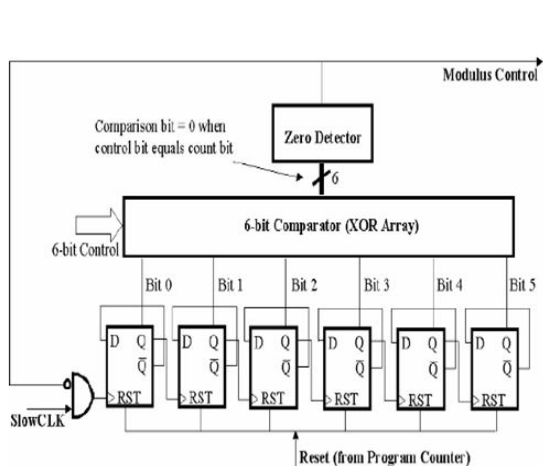


Fig 4: Swallow (S) Counter

II. Programmable (P) Counter

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P 4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=0) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33 (N/(N+ 1)) or 64/65 (N/(N+ 1)) dual-modulus prescaler is used, a 7 bit P counter is needed for the low-frequency band (2.4 GHz) while an 8-bit S-counter would be needed for the high frequency band(5-5.825 GHz) with a fixed 5-bit S counter. Thus, the multimodulus32/33/47/48 or 64/65/78/79 prescaler eases the design complexity of the P-counter.

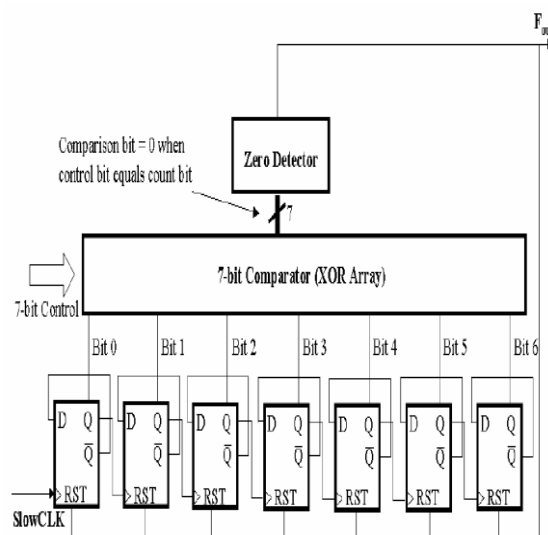


Fig 5: Programmable (P) Counter

VI. SIMULATION RESULTS

TABLE I
 PRESCALAR FREQUENCY DIVIDE RATIOS

Sel	MOD	MC	MODE
0	1	1	Divide-by-2
	0	1	Divide-by-2
	0	0	Divide-by-3
1	1	0	Divide-by-2
	1	1	Divide-by-3

1) When Sel='0':

When Sel='0' the output from NAND2 gate is given to the prescaler and the multimodulus prescaler selects 32/33 mode and the division ratio is controlled by MOD signal. When MOD=1 the output from NAND2 gate switches to logic' 1 ' and the prescaler operates in divide-by-2 for entire operation. i.e., now division ratio of 32 (N) is performed. Similarly when MOD = 0, MC remains high for first 30 input clock cycles and goes low for 3 input clock cycles. Thus division ratio of 33(N+ 1) is performed. N and N+ 1 are given by

$$N = (AD * N_1) = 32$$

$$N + 1 = ((AD - 1) * N_1) + (1 * (N_1 + 1)) = 33$$

2) When Sel='1':

When Sel=1, the inverted output from NAND2 gate is given to the input of 2/3 prescaler and multimodulus prescaler operates in 47/48 mode. MOD signal controls the division ratio. When MOD=1 and MC=1 prescaler operated in divide-by-3 for the entire input cycles and division ratio of 48 (N+1) is performed. When MOD=1 and MC=0 divideby-2 is selected for entire input clock cycles for

prescaler and the division ratio of 47(N) is performed. N and N+1 are given by

$$N = ((AD - 1) * (N1 + 1)) + (1 * N1) = 47$$

$$N + 1 = (AD * (N1 + 1)) = 48$$

In order to get 64/65/78/79 clock cycles we need to operate 4/5 prescaler by making the control signal sel of second MUX to '1'. To get 32/33/47/48 prescaler, the second MUX should be equal to '0' means the control signal sel of the second MUX should be equal to '0' and to get 64/65/78/79 prescaler, the second MUX should be equal to '1' means the control signal sel of the second MUX should be equal to '1'

3) When Sel='0':

When Sel='0' the output from NAND2 gate is given to the prescaler and the multimodulus prescaler selects 64/65 mode and the division ratio is controlled by MOD signal. When MOD=1 the output from NAND2 gate switches to logic '1' and the prescaler operates in divide-by-2 for entire operation. i.e., now division ratio of 64 (N) is performed. Similarly when MOD = 0, MC remains high for first 62 input clock cycles and goes low for 3 input clock cycles. Thus division ratio of 65(N+ 1) is performed. N and N+ 1 are given by

$$N = (AD * N_1) = 64$$

$$N + 1 = ((AD - 1) * N_1) + (1 * (N_1 + 1)) = 65$$

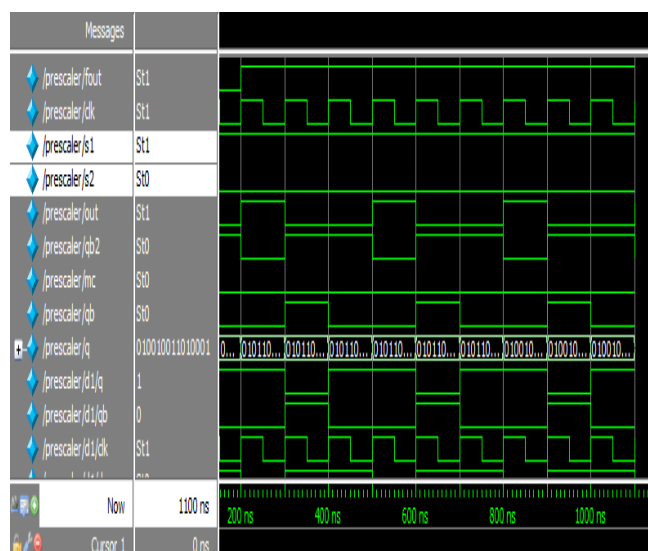
4) When Sel='1':

When Sel=1, the inverted output from NAND2 gate is given to the input of 2/3 prescaler and multimodal's prescaler operates in 78/79 mode. MOD signal controls the division ratio. When MOD=1 and MC=1 prescaler operated in divide-by-3 for the entire input cycles and division ratio of 79 (N+1) is performed. When MOD=1 and MC = 0 divideby-2 is selected for entire input clock cycles for prescaler and the division ratio of 78(N) is performed. N and N+1 are given by

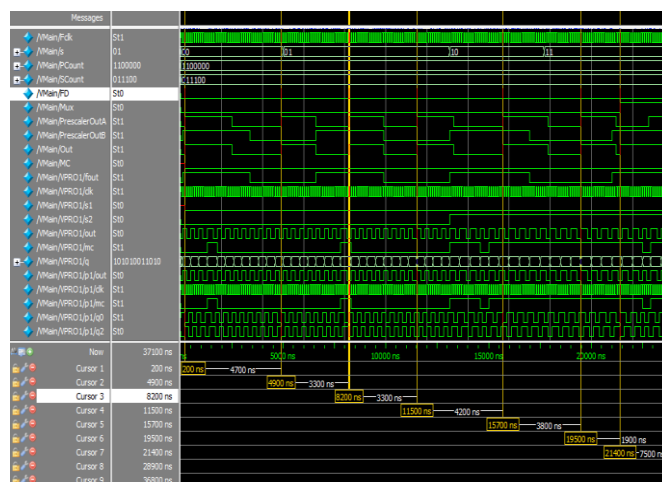
$$N = ((AD - 1) * (N1 + 1)) + (1 * N1) = 78$$

$$N + 1 = (AD * (N1 + 1)) = 79$$

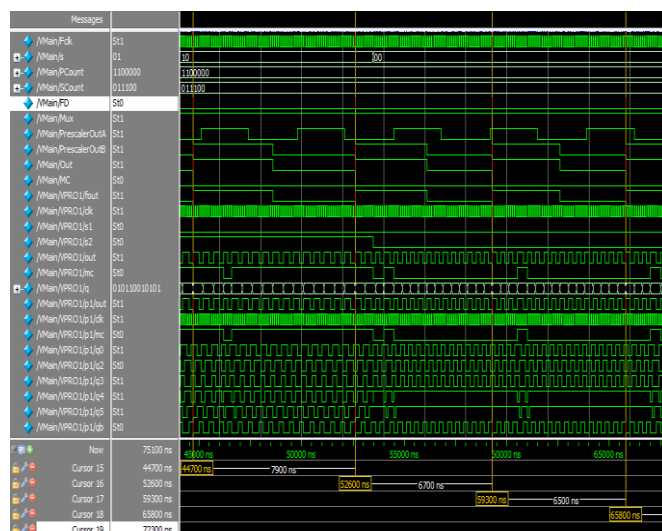
The results are shown below:



PRESCALER 2/3



DIVIDE BY 32/33/47/48



DIVIDE BY 64/65/78/79

VII. CONCLUSION

In this paper a simple approach for the low power multiband clock distribution using single phase clock distribution for Wireless Local Area Networks frequency synthesizer is presented. In this project, a wideband 2/3 or 4/5 prescaler is verified by the design of modified wide band multimodulus 32/33/47/48 or 64/65/78/79 prescaler. A dynamic logic multiband flexible integer N divider is designed which uses the wide band 2/3 prescaler, multimodulus 32/33/47/48 or 64/65/78/79 prescaler. The technique for low power fully programmable divider using design of reloadable bit cells for P and S Counter is given. P and S counters can be programmed accordingly for the required bands of frequencies, so that it provides solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4 and IEEE 802.11 a/b/g WLAN applications with variable channel spacing. In this paper we worked on the four modes like 32/33, 47/48, 64/65 and 78/79 prescaler. The future work will be combining wide band 2/3 prescaler, 4/5 prescaler and 8/9 prescaler to provide six modes of operations like 32/33, 47/48, 64/65, 78/79, 128/129 and 143/144. This means a wide band 2/3 or 4/5 or 8/9 prescaler is verified by the design of multimodulus 32/33/47/48 or 64/65/78/79 or 128/129/143/144 prescaler in future work. So future flexible divider controls more number of frequency bands.

REFERENCES

- [1] Vamshi Krishna Manthana, Manh Anh Do, Chirn Chye Boon, and Kiat Seng Yeo "A Low-Power Single-Phase Clock Multiband Flexible Divider" , IEEE transactions on very large scale integration (VLSI) systems, vol. 20, no. 2, February 2012.
- [2] H.R.Rategh et al., "A CMOS frequency synthesizer with an injected locked frequency divider for 5-GHz wireless LAN receiver," IEEE J. Solid-State Circuits, vol. 35, no. 5, pp. 780-787, May 2000.
- [3] P. Y. Deng et al., "A 5GHz frequency synthesizer with an injection locked frequency divider and differential switched capacitors," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 2, pp. 320-326, Feb. 2009.
- [4] L. Lai Kan Leung et al., "A 1-V 9.7-mW CMOS Frequency synthesizer for IEEE 802.11a transceivers," IEEE Trans. Microwind. Theory Tech., vol. 56, no. 1, pp. 39-48, Jan. 2008.
- [5] M. Alioto and G. Palumbo, Model and Design of Bipolar and MOS Current-Mode Logic Digital Circuits. New York: Springer, 2005.

- [6] Y. Jorgen etc all, "A true single-phase-clock Dynamic CMOS circuit technique," IEEE J. Solid-State Circuits, vol. 24, no. 2, pp. 62-70, Feb. 1989.
- [7] S. Pellerano etc, "A 13.5-mW 5 GHz frequency synthesizer with dynamic-logic frequency divider," IEEE J. Solid-State Circuits, vol. 39, no. 2, pp. 378-383, Feb. 2004
- [8] V. K. Manthana et al., "A low power fully programmable J MHz resolution 2.4 GHz CMOS PLL frequency synthesizer," in Proc. IEEE Biomed. Circuits Syst. Conf, Nov. 2007.pp 187-19.
- [9] X.P.Y u et al., "Design and optimization of the extended true single phase clock based prescaler", IEEE Trans. Microw. Theory Tech., vol.56, no. 11, pp.3828-3835, Nov.2006.
- [10] X.P.Y u et al., "Design of a low power wideband high resolution programmable frequency divider", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol.13, no. 9, pp.1098-1103, Sep.2005.